

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application Serial No.: TBA

Filed: CONCURRENTLY HERewith

For: **INTEGRATED CIRCUIT DEVICES HAVING BARRIER LAYERS BETWEEN
UPPER ELECTRODES AND DIELECTRIC LAYERS AND METHODS OF
FABRICATING THE SAME**

Date: 03/18/2004

Mail Stop PATENT APPLICATION
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

INFORMATION DISCLOSURE STATEMENT

Sir:

Attached is a list of documents on form PTO-1449 together with a copy of each identified document. It is requested that these documents be considered by the Examiner and officially made of record in accordance with the provisions of 37 C.F.R. §1.56 and Section 609 of the MPEP.

No fee is believed due. However, the Commissioner is hereby authorized to charge any deficiency or credit any overpayment to Deposit Account No. 50-0220.

Respectfully submitted,



Elizabeth A. Stanek
Registration No. 48,568


Myers Bigel Sibley & Sajovec, P.A.
P. O. Box 37428
Raleigh, North Carolina 27627
Telephone: (919) 854-1400
Facsimile: (919) 854-1401
Customer No. 20792

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Ban Youhan

Date of Signature: **03/18/2004**

FORM PTO-1449 U.S. Department of Commerce Patent and Trademark Office LIST OF DOCUMENTS CITED BY APPLICANT (Use several sheets if necessary)				Attorney Docket Number: 5649-1188		Serial No.: To Be Assigned	
				Applicants: Jung-hee Chung et al.			
				Filing Date: Concurrently Herewith		Group:	
U. S. PATENT DOCUMENTS							
Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date if Appropriate
FOREIGN PATENT DOCUMENTS							
		Document Number	Date	Country	Class	Subclass	Translation Yes No
	1	10-0297100	11/1/2001	KR			Abstract
	2	7-14992	1/17/1995	JP			Abstract
OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)							

Examiner Signature		Date Considered	
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*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.